CLAIMS

I claim:

1. An apparatus comprising:

a storage device to receive incoming data; and

a select circuit to select between a first strobe to strobe in the incoming data at a first strobe rate and a second strobe to strobe in the incoming data at a second strobe rate.

2. The apparatus of claim 1, wherein the select circuit is a multiplexer.

3. The apparatus of claim 1, wherein the select circuit is to receive a select signal from a value stored in a register.

4. The apparatus of claim 1 further including a register to store a programmable value used to select between the first and second strobes.

5. The apparatus of claim 1, wherein the storage device is a first-in, first-out (FIFO) buffer to receive incoming data to be buffered for transfer onto a data bus having different timing than the first or second strobe rate.

6. The apparatus of claim 5, wherein the FIFO is comprised of latches to latch in the data and output pairs of bits based on timing of the data bus.

7. The apparatus of claim 5, wherein the FIFO is comprised of four latches to strobe in four bits of data and output a pair of bits onto the data bus during a first portion of a clock cycle and another pair of bits during a second portion of the clock cycle.

8. The apparatus of claim 5 further including a second select circuit disposed in a data path of the incoming data to introduce delay in the data path to maintain phase relationship between the incoming data and the first or second strobe selected.

9. An integrated circuit comprising:

an interim first-in, first-out (FIFO) buffer to strobe in data from a memory based on a first strobe signal or a second strobe signal, the strobe signals based on a configuration of the memory to be used to store the data; and

a select circuit to select between the first strobe signal and the second strobe signal, the first and second strobe signals to have different strobe rates to strobe in the data from the memory.

10. The integrated circuit of claim 9, wherein the select circuit is a multiplexer.

11. The integrated circuit of claim 10, wherein the multiplexer is to receive a select signal from a value stored in a register.

12. The integrated circuit of claim 10 further including a register to store a programmable value to be used by the multiplexer to select between the first and second strobe signals.

13. The integrated circuit of claim 10, wherein the FIFO is comprised of latches to latch in the data and output pairs of bits based onto an internal data bus based on timing of the data bus.

14. The integrated circuit of claim 10, wherein the FIFO is comprised of four latches to strobe in four bits of data and output a pair of bits onto an internal data bus during a first portion of a clock cycle and another pair of bits during a second portion of the clock cycle.

15. The integrated circuit of claim 10 further including a second multiplexer disposed in a data path of the incoming data to introduce delay in the data path to maintain phase relationship between the incoming data and the first or second strobe selected.

16. A method comprising:

generating a plurality of strobes;

selecting one strobe from the plurality of probes; and

receiving incoming data using the selected strobe.

17. The method of claim 16 further including multiplexing the plurality of strobes and using a select signal for selecting the one strobe.

18. The method of claim 17 further including delaying the incoming data to maintain phase relationship between the incoming data and the selected one strobe.

19. The method of claim 18, wherein the receiving incoming data includes latching in the data and outputting pairs of bits based onto an internal data bus based on timing of the data bus.

20. The method of claim 18, wherein the receiving incoming data includes latching to strobe in four bits of data and outputting a pair of bits onto an internal data bus during a first portion of a clock cycle and another pair of bits during a second portion of the clock cycle.